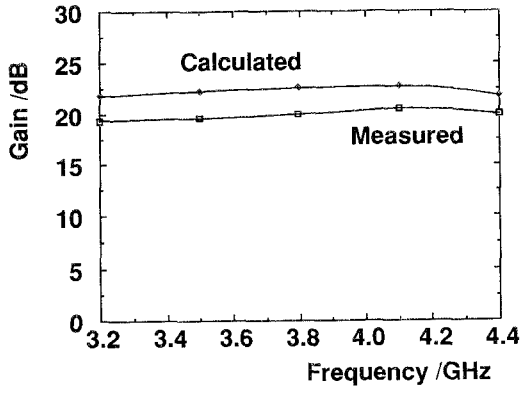

Fig. 3. Performance of the amplifier.

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The authors are indebted to Ms. T. H. Wang for amplifier fabrication and measurement, and to Prof. Y. S. Wu for encouragement and support.

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X-Band Low Phase Distortion MMIC Power Limiter

T. Parra, Jm. Dienot, M. Gayral, M. Pouysegur, Jf. Sautereau, and J. Graffeuil

***Abstract*—This paper describes the design and performance of a 8 GHz MMIC MESFET power limiter. This limiter incorporates a special gate biasing scheme and makes use of appropriate load conditions which reduce the unexpected phase variations experienced by the signal through the device.**

Measured performances (phase variations less than 8° over a 22 dB input power range) are found to be in agreement with the theoretical ones obtained from large signal simulations.

I. INTRODUCTION

Microwave power limiters are required for signal processing under constant amplitude conditions, for example to suppress AM components before demodulation of a microwave FM signal or to insure the incoming signal to a receiver does not exceed a given threshold. So far, this function has been fulfilled with p-i-n diodes, but this is not suitable for building MMIC since these diodes are not yet available from commercial foundries. Then GaAs FET limiters have been introduced [1] additionally providing a good input-output isolation.

The basic idea is to utilize the output power saturation of a class A GaAs FET amplifier. The FET is operated beyond its compression point so that the output RF signal cannot exceed its saturation level whatever the input signal amplitude. Over an input power dynamic range, output power variations may be reduced by cascading several FET stages [2].

The aforementioned applications require a low AM to PM conversion. Unfortunately the phase shift introduced by the limiter depends on the amplitude of the RF signal. Similarly the maximum range $\Delta\Phi$ of the observed phase shift variations (phase distortion) may greatly vary from 20° on some devices to a mere 1° on others, for a given power range.

The analysis of this phenomenon has been already reported [3] and the first section of this paper summarizes the most significant results. Then the second section describes a large signal model which yields input-output phase variations in good qualitative agreement with the experiment. Finally these two sections support the design of a low phase distortion MMIC power limiter whose characteristics are measured.

II. PHASE SHIFT DISTORTION ORIGINS

The results concerning the phase shift distortion origins are presented [3]. It has been shown that phase shift variations are mostly related to large input capacitance variations at moderate power levels and that at higher levels they are related to the forward-biased gate during a fraction of the RF cycle.

We therefore proposed the addition of an external series resistor, Rg, in the gate bias supply circuit [4]. This resistor shortens the fraction of the RF cycle during which the gate is forward biased and

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T. Parra, Jm. Dienot, M. Gayral, Jf. Sautereau, and J. Graffeuil are with LAAS-CNRS and Université Paul Sabatier, 7 Ave du Colonel Roche, 31077 Toulouse Cedex, France.

M. Pouysegur is with Alcatel Espace 126 Ave JF. Champollion, 31037 Toulouse Cedex, France.

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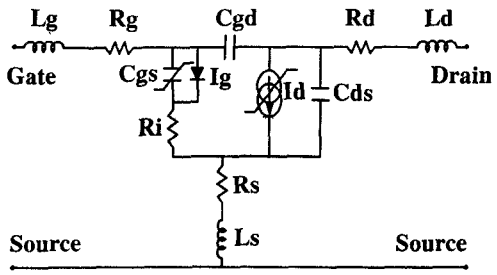


Cgs(pF) (4th degree polynomial)

C0	C1	C2	C3	C4
35	14	.03	12	.05

Igs(μA)

Is	α
36.3	18

Ids(A) (Tajima expression)

τ	Idss	Vpo	Vdsp	Vphi	A	B	M	P	W
3.1E-12	117E-3	1 2	6	.8	.8	5 9E-5	.5	1	1.4E-4

Fig. 1. Large signal equivalent circuit of a probe tested MESFET. Linear elements are obtained from S parameter measurements (40 MHz–20 GHz) and nonlinear elements from pulsed current-voltage and 10 MHz capacitance-voltage measurements.

providing its value is correctly set, thus decreases the introduced phase shift distortion at higher power levels. In practice, a good approximation is found for the optimum value of Rg:

$$Rg = Ro.\left(\frac{400}{Z}\right)$$

where Z is the gate width in micrometers and Ro equals 20 Ω.

The introduced phase shift distortion can additionally be minimized by slightly modifying the transistor output match. This tuning optimizes the load-line slope in order to restrict once again the fraction of the RF cycle corresponding to a forward biased gate.

All these methods can be easily applied to monolithic implementations. To substantiate these statements, we have designed a low phase distortion MMIC power limiter.

III. Large Signal Modeling and Simulations

An appropriate MESFET nonlinear model topology is presented in Fig. 1. The first nonlinearity is the dependent drain current generator $Id(Vgs, Vds)$ which has been expressed following Tajima [6] expression $Id = f(Vgs, Vds)$. The different parameters involved in this expression are obtained from the fit of pulsed $Id(Vgs, Vds)$ measurements to prevent any thermal or trapping problems [7].

Since phase distortion is mostly related to the gate capacitance nonlinearity, two additional nonlinearities are considered in the model. The first nonlinearity concerns the gate diode current and accounts for the forward conduction. Its expression is the usual expression $Ig = Is.[\exp(\alpha Vgs) - 1]$ in which parameters Is and α are also derived from pulsed measurements. The second one consists of the distributed gate-source capacitance Cgs. The expression of the depletion capacitance of a uniformly doped Schottky diode is often used to describe the variations of Cgs versus Vgs and Vds but is not good enough in terms of accuracy. A certain number of attempts at drawing up more accurate capacitance models were therefore performed [8]–[10] usually involving an almost two-dimensional analysis assuming uniform doping. However a closed-form of the gate charge versus Vgs is required as in most nonlinear simulators, in addition to the capacitance formula. The difficulties in obtaining this analytical expression in most models led us to the selection

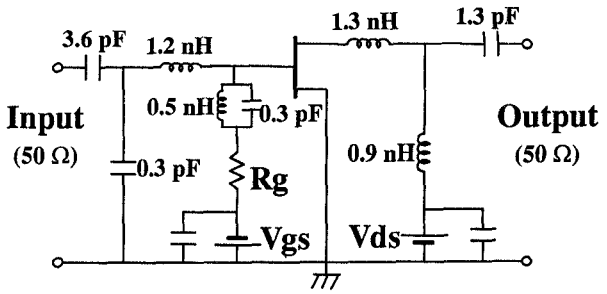


Fig. 2. Implemented topology of a one stage MMIC power limiter.

of a polynomial relationship. The coefficients are obtained from measurements of $Cgs(Vgs, Vds)$ using an impedance analyzer at 10 MHz. Then the charge $Qgs(Vgs, Vds)$ was easily obtained for integrating the capacitance expression.

Usually, the gate-drain capacitance Cgd is small and little dependent on bias voltage so that it can be kept constant.

Finally the value for Cgd and other linear parameters of the model were determined from additional static and S parameter characterizations.

IV. Low Phase Distortion GaAs FET Monolithic Power Limiter

A. Circuit Design

Fig. 2 shows the topology of the MMIC limiter circuit. The FET used features a 6 × 50 μm wide gate delivering a level of saturation power, corresponding to the maximum output power for the MMIC limiter, of 12 dBm under a 3 V drain-source bias voltage and a drain current of $Idss/3$. Input and output matching circuits were first optimized using a linear simulator (MDS of Hewlett Packard) in the frequency band 7.9–8.4 GHz in order to achieve a maximum small signal gain yielding a sufficiently constant output power with a minimum number of cascaded FET stages. For stable operation an antiresonant circuit with a series resistance (20 Ω in that case) was placed at the FET input. The gate was biased through this circuit branch in which the same resistance was equally used for phase distortion minimization.

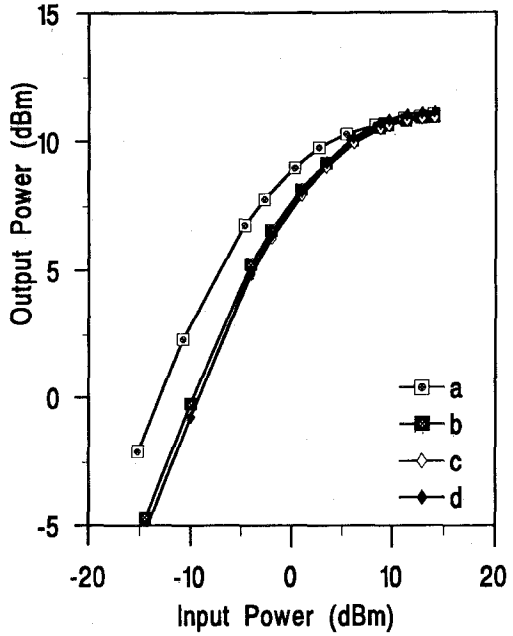
Once the lumped elements of the matching networks had been obtained nonlinear simulations were performed. The output circuit and the gate biasing circuit resistance value had to be optimized relative to phase distortion using a dedicated software. The nonlinear simulator used for these simulations (LIMHA, developed by IRCOM Limoges [5]) is based on the harmonic balance method. A minimum phase shift was thus obtained for a given input power range.

The results of this optimization are reported in Fig. 3. It clearly appears that for an input power range of 30 dB the initial 16° phase distortion is lowered to less than 2° with a 9 dB small signal gain value.

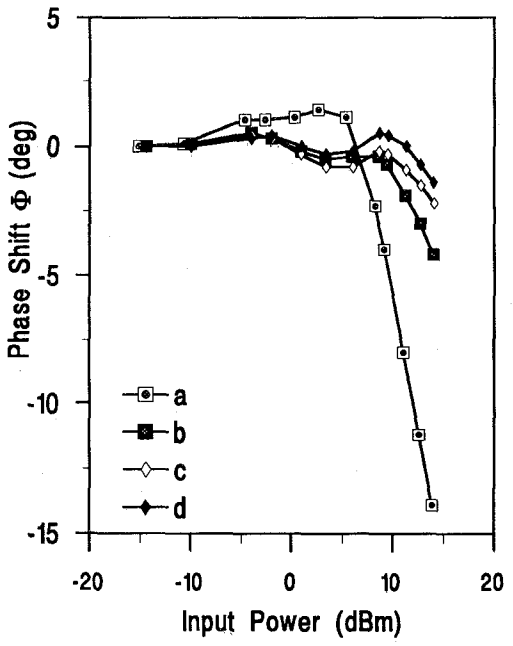
A new linear simulation is then performed to check that the gain and the VSWR are not too much damaged in the considered frequency band. The results are displayed in Fig. 4 and show that the small signal VSWR IN and OUT are less than −20 dB at 8.2 GHz. The circuit was then processed using a commercial foundry.

B. Measured Results

Fig. 5 shows the top view of the power limiter chip. The 1 mm × 1 mm chip includes two one-stage limiters that may be cascaded by wire bonding.



(a)



(b)

Fig. 3. Nonlinear simulation results. Output power characteristics (Fig. 3(a)) and phase shift variations (Fig. 3(b)) are represented versus input power for each step of the nonlinear optimization ($f = 8.1$ GHz). Curves (a): input and output matching circuits achieving maximum small signal gain value. Curves (b): matching conditions of curve (a) plus a 15 Ω external gate resistor. Curves (c): matching conditions of curve (a) plus a 20 Ω external gate resistor. Curves (d): conditions of curve (c) plus a slight detuning of the output matching circuit.

Each one-stage limiter was tested using a wafer probe station and the experimental setup, used for large-signal phase distortion measurements, already described [3].

Fig. 6 shows the measured output power and phase shift characteristics versus input power. It can be seen that, with an input power range of 22 dB (−13 dBm to +9 dBm), the phase distortion of the monolithic limiter is less than 8°. If these results are compared to

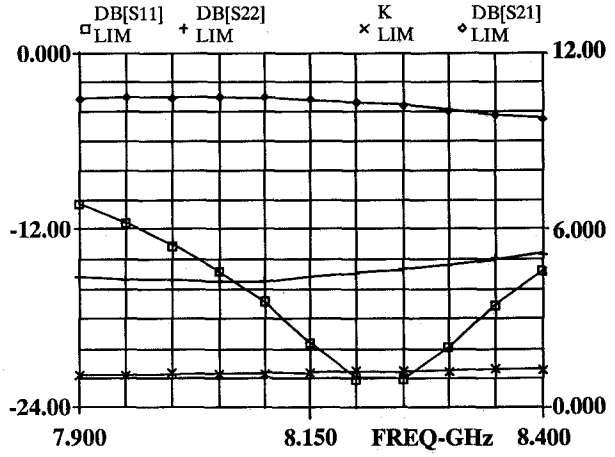


Fig. 4. Simulated linear characteristics of a one-stage optimized limiter: □ input return loss (dB); + output return loss (dB); × stability coefficient; ◇ transmission coefficient (dB).

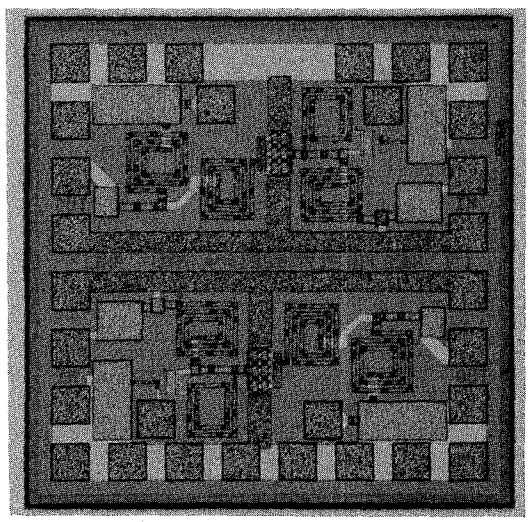


Fig. 5. MMIC power limiter chip.

what was expected from the nonlinear simulation a fair agreement is obtained up to a 0 dBm input power and between 0 dBm and +9 dBm the observed difference increases up to 6°. This discrepancy could be due to inaccuracies in our nonlinear model: this model was actually achieved with measurements on a set of ten MESFETs from the same foundry run, so that process variations between runs have not been included in our model. However, the observed phase shift is not so large as to rule out the use of these limiters in future applications. By assuming moreover that the maximum allowed forward gate current is 1 mA, it was found that the maximum safe input power level for the limiter is about 15 dBm (gate width 300 μ m).

V. Conclusion

In this paper, the design and measured performance of a monolithic power limiter have been reported. The designed monolithic power limiter exhibits a small gain of 8 dB, an output power of 12 dBm and an 8° maximum phase distortion over a 22 dB input power range.

In addition, our work has shown that a nonlinear function can be designed with a reasonable level of accuracy without fine-tuning of the circuit after processing. The accuracy of the performance and the ease of design could nevertheless be increased with foundries able to furnish a more complete FET characterization, including

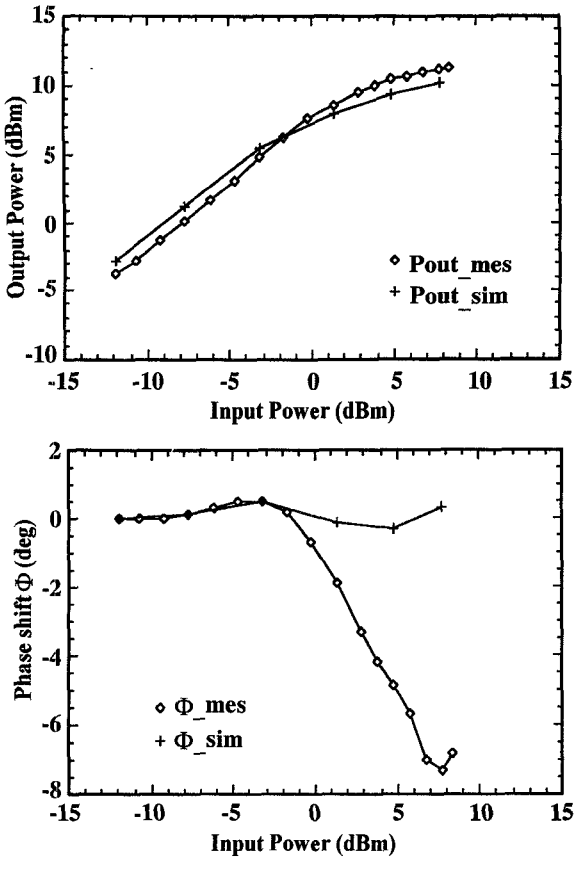


Fig. 6. Measured output power and phase shift versus input power of a low phase distortion MMIC limiter.

gate-source capacitance $Cgs(Vgs, Vds)$ measurements and current-voltage characteristics measured under pulsed conditions.

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Breakdown in the Inhomogeneous Electric Field of a Microwave Transmit-Receive Switch

V. Semenov, D. Anderson, and M. Lisak

***Abstract*—A detailed analytical investigation is made of the threshold for breakdown in microwave transmit-receive switches. The geometry of the keep alive contacts of the switch is modelled as a double cone configuration and the subsequent diffusion equation for the electron density in the presence of strongly inhomogeneous ionization is solved analytically. Predictions for the breakdown power are found to be in agreement with previously presented experimental results.**

I. INTRODUCTION

Breakdown of gases in non-uniform microwave fields has a number of important applications ranging from breakdown in microwave cavity modes [1], [2] to breakdown in the strongly inhomogeneous near fields of antennas [3], [4] and around conducting obstacles in wave guides or cavities [5]–[7]. In the presence of a spatially inhomogeneous microwave field, the concomitant ionization of the gas varies with position and the corresponding diffusion equation determining the break-down properties of the gas becomes complicated. This is particularly so when the field localization region is much smaller than the ionization region, cf. [8]. An interesting and technically important example of this situation occurs in microwave transmit-receive (TR) switches where the strongly localized electric field enhancement created by the sharp conical keep alive contacts significanly lower the power level needed to initiate the breakdown process, cf. [9].

A consistent determination of the breakdown level in the TR-switch is made difficult by two complicating factors: (i) the details of the spatial variation of the electric field enhancement in the vicinity of the contacts are not known and (ii) the geometry of the diffusion process makes the determination of the characteristic diffusion length difficult. In [9], a rough estimate of the average field enhancement and the effective diffusion length were made and the predicted breakdown level could be made to agree with experimental results. In the present work we will give a more detailed and self consistent analysis of the breakdown threshold for TR-switches by analyzing an idealized problem which models the main features of the switch, viz. the spatially varying ionization and the conical diffusion geometry.

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The authors are with the Institute for Electromagnetic Field Theory, Chalmers Univ. of Technology, S-412 96 Göteborg, Sweden. V. Semenov's permanent address is the Institute of Applied Physics, USSR Academy of Sciences, 46 Ulyanov Street, Nizhny Novogorod 603600, USSR.

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